Amendments to the Specification

Please replace the paragraph on page 1 beginning at line 11 with the following new paragraph:

Generally, in a DS/CDMA communication system, a receiver is required to synchronize (Psuedo-Noise) PN sequences prior to detection of data. Mostly, the PN sequence synchronization is performed by two steps of code acquisition and code tracking in sequence. Here, regarding the code acquisition, research for a high-speed acquisition technique to shorten the acquisition time has been made with great interest and anxiety.

Please replace the paragraph on page 5 beginning at line 9 with the following new paragraph:

The state signal r(t) having arrived at the receiving part is despread by 2^b quadrature symbol correlators, integrated for a symbol time with integrators 60, 61 and 62, and then converted into input values $|Y_j|$ (j=0,1,...,2b-1) of the 2^b decision logic circuits by taking their absolute values. In the actual implementation, the absolute value is generally obtained via absolute value units 63, 64 and 65 by multiplying the in-phase (I-phase) value and the quadrature-phase (Q-phase) value of the output of the integrating section and then obtaining a square root value thereof. At this time, the correlation signal used for correlating with the state signal in the j-th quadrature symbol correlator is a conjugate complex signal of the spread quadrature signal $m_j(t)$, that is obtained by multiplying the quadrature symbol signal $s_j(t)$ and the igniter sequence signal c(t) used for the quadrature modulation in the

transmitting part. The value $|Y_j|$ (j=0,1,..., 2b-1) are then input to the decision logic section 69.

Please replace the paragraph on page 5 beginning at line 19 and bridging page 6 with the following new paragraph:

Figures 2A and 2B illustrate the operation of the decision logic ~~circuit~~ section 69 in Figure 1. The decision logic circuit operates differently in the igniter sequence acquisition mode and in the state sample detection mode. In the igniter sequence acquisition mode (i.e., the step prior to the igniter sequence acquisition), the maximum value among the 2^b input values $|Y_j|$ (j=0,1,...,2^b-1) is compared with the predetermined threshold value R_0. If the maximum value is larger than the threshold value, the decision logic circuit declares the sequence phase consistent state H_1, and goes to the acquisition confirmation step. If the maximum value is smaller than the threshold value, the decision logic circuit declares the sequence phase discrepant state H_0, and checks whether the next sequence phase is consistent.

Please replace the paragraph on page 6 beginning at line 9 with the following new paragraph:

In the state sample detection mode (i.e., the step after the igniter sequence acquisition), the decision logic circuit determines which value is the maximum value among

the 2^b input values $|Y_j|$ ($j=0,1,\ldots,2^b-1$), and detects the corresponding quadrature state symbol ~~s_j~~ $\underline{S_j}$. This state symbol is demapped by b state samples.

Please replace the paragraph on page 12 beginning at line 10 with the following new paragraph:

The preferred embodiment performs a high-speed discrimination and acquisition of the long-period PN sequences by applying the D^2SA technique to the next-generation DS/CDMA system, and ~~solve~~ <u>solves</u> the uncertainty problem of the channel estimation, which is caused by the pilot signal generated due to the use of the DPSK modulation in the base station, by the pre-rotation of the data constellation as well.

Please replace the paragraph on page 15 beginning at line 4 with the following new paragraph:

The sample spreading section 20 of the transmitter preferably includes a PSK symbol mapping section 21 for mapping the state samples outputted from the time-advanced parallel sampling section 13 onto a code symbol and outputting a corresponding PSK symbols ~~X_n,~~ $\underline{X_n}$. It also preferably includes the DPSK encoding section 22 for encoding the DPSK symbols f_n by adding the phase integrated until the previous symbol time to the phase of the PSK symbol X_n outputted from the PSK symbol mapping section 21. Additionally, it preferably includes the igniter SRGs 24 and 25 for generating igniter sequences to spread the generated DPSK symbols f_n, and a spreader 23 for spreading the DPSK symbols f_n by the complex igniter sequence and outputting the state signal.

Please replace the paragraph on page 15 beginning at line 12 with the following new paragraph:

The receiver illustrated in Figure 3B preferably includes the sample despreading section 30 for acquiring the corresponding igniter sequence from the state signal outputted from the sample spreading section 20, despreading the input state signal by the acquired igniter sequence, and ~~modulating~~ <u>demodulating</u> the despread state signal. It also preferably includes the DSA despreading section 40 for synchronizing the transmitter/receiver sequence generators by comparing state sample values of its own sequence generator that generates one or more main sequences with the state sample values demodulated by the sample despreading section 30, and despreading and descrambling the spread user data by a descrambling sequence generated using the main sequence corresponding to the synchronization timing. Next, the receiver also preferably includes a channel estimator 50 for estimating a channel gain and a carrier phase by multiplying a value obtained by DPSK-encoding the state sample values for the sequence generator of the DSA despreading section 40 by a value obtained by multiplying the encoded output by the state signal despread by the sample despreading section 30, and then multiplying a multiplied value by a low-pass-filtered value.

Please replace the paragraph on page 18 beginning at line 18 bridging page 19 with the following new paragraph:

The depletion encoding section 53 preferably comprises a PSK symbol mapping section 51 for mapping the state samples outputted from the parallel sampling section 45 of the DSA despreading section onto the respective complex symbols and outputting the state symbol Xn which is the corresponding PSK symbol, and an encoding section 56 for producing the DPSK symbol Fn by adding the phase integrated until the previous symbol time to the phase of the PSK symbol Xn. The high-speed cell searching apparatus using the D^2SA technique according to the present invention will be described with reference to Figures 3A and 3B.

Please replace the paragraph on page 20 beginning at line 6 with the following new paragraph:

The ~~QPSK~~ PSK symbol mapping section 21 maps the two provided state samples onto the respective complex symbols and outputs corresponding state symbols X_n which are the PSK symbols.

Please replace the paragraph on page 20 beginning at line 9 with the following new paragraph:

Then, the block following the ~~QPSK~~ PSK symbol mapping section 21 performs the DPSK encoding. At this time, DPSK symbols f_n are generated by adding the phase, integrated through the previous symbol time, to the phase of the PSK symbols X_n.

Please replace the paragraph on page 22 beginning at line 1 with the following new paragraph:

The received state signal is despread by the igniter sequence generated by the igniter SRGs 32 and 33, and then correlation-integrated via an integrator 101, absolute value unit 101 and square root value 102

Please replace the paragraph on page 23 beginning at line 1 with the following new paragraph:

After the igniter sequence discrimination and synchronization is completed, an accurate chip timing is estimated using the noncoherent delay-locked loop (DLL) illustrated in Figure 4B. Further, Figure 4B also illustrates despreaders 31a, 31b; correlation sections 201, 203; integrators 202, 204; vcc 206; and loop filter 205.